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09/585,263	06/02/2000	Donald F. Gordon	SEDN/070CIP4	5643
56015 7590 06/11/2007 PATTERSON & SHERIDAN, LLP/ SEDNA PATENT SERVICES, LLC 595 SHREWSBURY AVENUE SUITE 100 SHREWSBURY, NJ 07702			EXAMINER SALTARELLI, DOMINIC D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/585,263
Filing Date: June 02, 2000
Appellant(s): GORDON ET AL.

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Technology Center 2600

Gordon et al
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 20, 2007 appealing from the Office action mailed September 21, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,986,650	ELLIS ET AL	11-1999
5,485,197	HOARTY	01-1996

5793364	BOLANOS ET AL	08-1998
5,951,639	MACINNIS	09-1999

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1, 2, 5, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellis et al. (5,986,650) [Ellis].

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of Hoarty (5,485,197).

Claims 9, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of Bolanos et al. (5,793,364) [Bolanos].

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of MacInnis (5,951,639).

(10) Response to Argument

Rejection of Claims 1, 2, 5, and 8 under 35 U.S.C. 102(e)

First, appellant argues that Ellis fails to disclose generating and encoding the bitmaps at the headend, referring to the bit maps disclosed by Ellis as 'downloadable' (appeal brief, page 13) and thus not necessarily originating from the headend.

In response, there is an important distinction between appellants characterization of Ellis and what is actually stated by Ellis. Specifically, col. 6, lines 28-34 state:

When the schedule system is operating, as discussed in greater detail hereinbelow, the microcontroller 16 takes the program schedule

information stored in the DRAM 18 and, in conjunction with other **downloaded** data types such as stored bit maps for the screen configuration and the graphic symbol or logo displays stored in non-volatile memory 20 or, alternatively, in DRAM 18..." *[emphasis added]*.

Ellis clearly states here the bit map data has been **downloaded** along with the program schedule information, in addition to several other unnamed data types, which comprise the data stream provided to the receiver from the data provider (Ellis, col. 4, lines 55-67). Further, the section cited by appellant regarding the 'downloading' of bit map data into memory (Ellis, col. 5, lines 45-51) is further support for stating that bit map data originates from the headend, as this section is referring to updating of application software in a receiver (see Ellis, col. 5, lines 36-65), and if appellant wishes to assume said application software includes the bit maps in question, Ellis also clearly states that application data is delivered to the receiver from the head end (see Ellis, col. 5, lines 11-16, where the program guide data and application data are received over input line 11, which originates from the headend [data provider], see Ellis, col. 4, lines 55-67).

Second appellant argues that, even if the bit maps originate from the headend, Ellis does not teach encoding the bit maps at the headend, stating that Ellis teaches merely modulating data with an analog signal (appeal brief, page 14).

In response, it must first be noted that the appellant has yet to provide a clear definition of what is meant by the term 'encoding' in the claim, thus far

having only made arguments to the effect of what encoding is not. The common definition of the term is simply "the process of putting a sequence of characters into a special format for transmission or storage purposes." For example, QPSK modulation is a method of transforming digital data into a special format for transmission purposes (see Ellis, col. 5, lines 11-16, wherein received data has been QPSK modulated). This also addresses the issue raised by appellant concerning what was identified as an inherency argument in the advisory action mailed on December 6, 2006. QPSK modulation is inherently a form of encoding, using individual symbols to represent two bits of data per symbol, and is expressly taught by Ellis as a means by which data is delivered to the receiver from the headend.

Rejection of Claim 7 Under 35 U.S.C. 103(a)

Here, appellant relies upon the patentability of claim 5, from which claim 7 depends, and thus relies upon the arguments presented above.

Rejection of Claims 9, 10, and 13 Under 35 U.S.C. 103(a)

Here, appellant restates the arguments regarding the Ellis reference presented previously, and are addressed above.

Rejection of Claim 14 Under 35 U.S.C. 103(a)

Art Unit: 2623

Here, appellant relies upon the patentability of claim 1, from which claim 14 depends, and thus relies upon the arguments presented above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dominic Saltarelli



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